DIAMOND SYSTEMS CORPORATION

ONYX-MM-DIO-XT

PC/104 Digital I/O Module

User Manual V1.4

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1. General Information and Features

ONYX-MM-DIO is a PC/104-compliant I/O module with 48 digital I/O lines. It is an 8-bit module, so it does not contain the 16-bit expansion bus connector. This connector is available as an option by requesting the –B16 suffix when ordering.

Two right-angle 50-pin (2x25) headers are provided for the I/O. J3, with 24 digital I/O lines, is on the right side of the module in the standard PC/104 I/O position. J4, with 24 additional digital I/O lines, is on the left side of the module. (The bottom edge of the module is defined as the edge with the PC/104 ISA bus connectors.)

All I/O signals are TTL compatible. The boards operate on +5V power supply only.

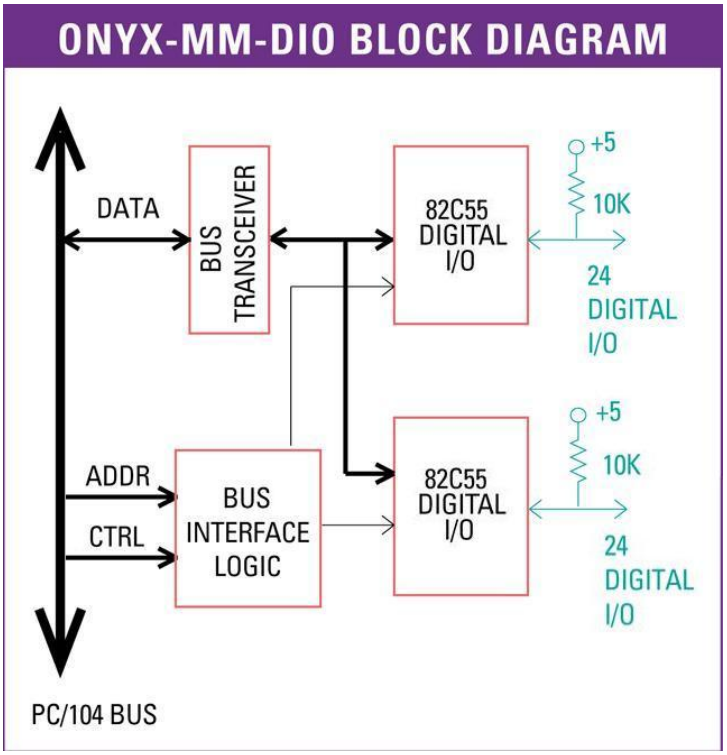
Digital I/O Features

48 TTL digital I/O lines are provided by 2 82C55 chips (24 per chip). Each line can source 2.5mA in a logic 0 state and sink 2.5mA in a logic 1 state. I/O lines are unbuffered, i.e. there is a direct connection between the 82C55 and the I/O header. Bit C0 of each 82C55 can be used to generate an interrupt on the PC bus (see **Interrupts** below).

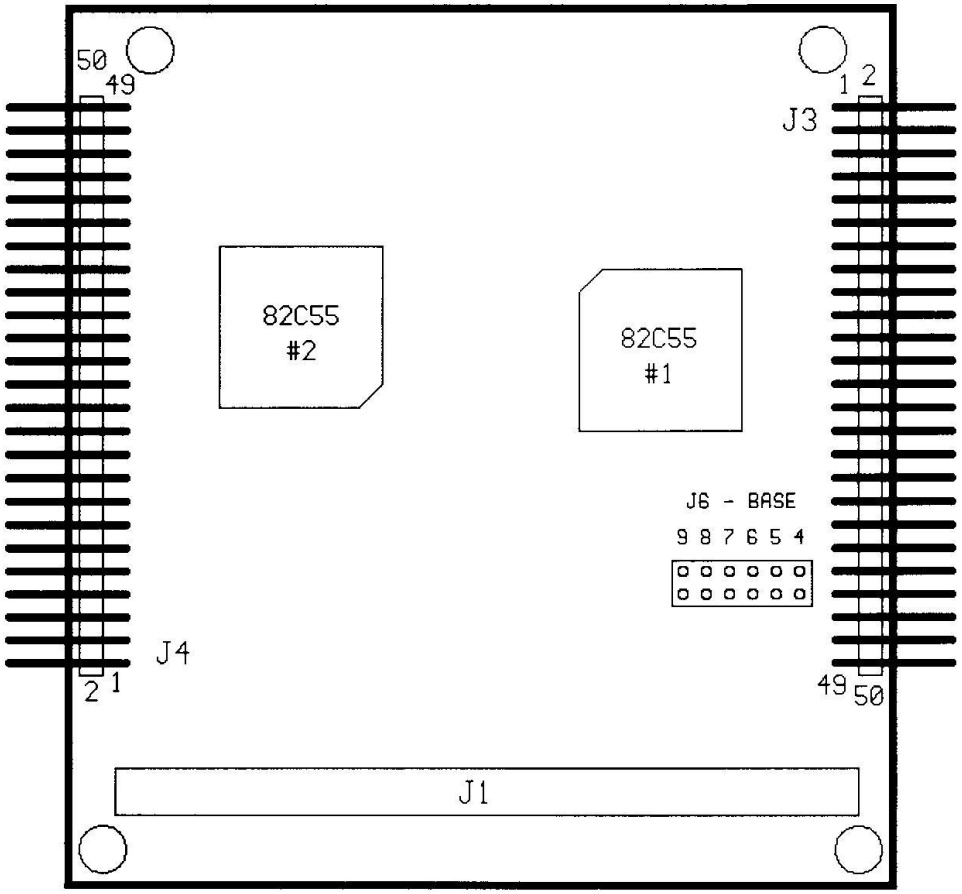
All digital I/O lines are connected to +5V through 10KΩ pull-up resistors.

Digital I/O lines are accessed through two 50-pin headers, J3 and J4, with 24 lines (one 82C55) on each header. See page 8 for I/O header pinouts.

Block Diagram



2. Onyx-MM-DIO Board Drawing



Item	Description
J1	PC/104 bus connector
J3	Digital I/O ports 1A, 1B, 1C
J4	Digital I/O ports 2A, 2B, 2C
J6	Board base address configuration

3. I/O Header Pinouts

J3: Digital I/O Header for 82C55 #1
J4: Digital I/O Header for 82C55 #2

Each of these headers is identical in pinout. They provide 24 digital I/O lines, +5, and ground. Pin 1 of J3 is in the upper right corner of the board, and pin 1 of J4 is in the lower left corner.

A7	1	2	Gnd
A6	3	4	Gnd
A5	5	6	Gnd
A4	7	8	Gnd
A3	9	10	Gnd
A2	11	12	Gnd
A1	13	14	Gnd
A0	15	16	Gnd
C7	17	18	Gnd
C6	19	20	Gnd
C5	21	22	Gnd
C4	23	24	Gnd
C3	25	26	Gnd
C2	27	28	Gnd
C1	29	30	Gnd
C0	31	32	Gnd
B7	33	34	Gnd
B6	35	36	Gnd
B5	37	38	Gnd
B4	39	40	Gnd
B3	41	42	Gnd
B2	43	44	Gnd
B1	45	46	Gnd
B0	47	48	Gnd
+5	49	50	Gnd

4. Base Address Configuration

ONYX-MM's base address is set with header J6, located at the lower right corner of the board. Each of the six pairs of pins on J6 corresponds to a different address bit. A pair left open is equal to a 1, and a pair with a jumper installed is equal to a 0. The header is used to select address bits 9-4, resulting in an 16-byte I/O decode. The leftmost pair selects address bit A9, and the rightmost pair selects address bit A4. Although any 16-byte location is selectable, certain locations are reserved or may cause conflicts. The table below lists recommended base address settings for ONYX-MM. The default setting is 300 Hex. "Open" means an open position, and "Inst" means a position with a jumper installed.

Base Address		**Header J6 Position**					
Hex	**Decimal**	**9**	**8**	**7**	**6**	**5**	**4**
220	544	Open	Inst	Inst	Inst	Open	Inst
240	576	Open	Inst	Inst	Open	Inst	Inst
250	592	Open	Inst	Inst	Open	Inst	Open
260	608	Open	Inst	Inst	Open	Open	Inst
280	640	Open	Inst	Open	Inst	Inst	Inst
290	656	Open	Inst	Open	Inst	Inst	Open
2A0	672	Open	Inst	Open	Inst	Open	Inst
2B0	688	Open	Inst	Open	Inst	Open	Open
2C0	704	Open	Inst	Open	Open	Inst	Inst
2D0	720	Open	Inst	Open	Open	Inst	Open
2E0	736	Open	Inst	Open	Open	Open	Inst
300	768 (Default)	Open	Open	Inst	Inst	Inst	Inst
330	816	Open	Open	Inst	Inst	Open	Open
340	832	Open	Open	Inst	Open	Inst	Inst
350	848	Open	Open	Inst	Open	Inst	Open
360	864	Open	Open	Inst	Open	Open	Inst
380	896	Open	Open	Open	Inst	Inst	Inst
390	912	Open	Open	Open	Inst	Inst	Open
3A0	928	Open	Open	Open	Inst	Open	Inst
3C0	960	Open	Open	Open	Open	Inst	Inst
3E0	992	Open	Open	Open	Open	Open	Inst

5. Register Map

Base +	**Function**	**Comments**
0	DIO port 1A	0 - 3 are 82C55 #1 registers
1	DIO port 1B	
2	DIO port 1C	
3	DIO port 1 configuration register	
4	DIO port 2A	4 - 7 are 82C55 #2 registers
5	DIO port 2B	
6	DIO port 2C	
7	DIO port 2 configuration register	

6. Register definitions

Base + 0: Digital I/O Register A, 82C55 no. 1

Bit	7	6	5	4	3	2	1	0
Name	1A7	1A6	1A5	1A4	1A3	1A2	1A1	1A0

1A7-1A0 Digital I/O port 1A, port A on 82C55 no. 1

Base + 1: Digital I/O Register B, 82C55 no. 1

Bit	7	6	5	4	3	2	1	0
Name	1B7	1B6	1B5	1B4	1B3	1B2	1B1	1B0

1B7-1B0 Digital I/O port 1B, port B on 82C55 no. 1

Base + 2: Digital I/O Register C, 82C55 no. 1

Bit	7	6	5	4	3	2	1	0
Name	1C7	1C6	1C5	1C4	1C3	1C2	1C1	1C0

1C7-1C0 Digital I/O port 1C, port C on 82C55 no. 1

Base + 4: Digital I/O Register A, 82C55 no. 2

Bit	7	6	5	4	3	2	1	0
Name	2A7	2A6	2A5	2A4	2A3	2A2	2A1	2A0

2A7-2A0 Digital I/O port 2A, port A on 82C55 no. 2

Base + 5: Digital I/O Register B, 82C55 no. 2

Bit	7	6	5	4	3	2	1	0
Name	2B7	2B6	2B5	2B4	2B3	2B2	2B1	2B0

2B7-2B0 Digital I/O port 2B, port B on 82C55 no. 2

Base + 6: Digital I/O Register C, 82C55 no. 2

Bit	7	6	5	4	3	2	1	0
Name	2C7	2C6	2C5	2C4	2C3	2C2	2C1	2C0

2C7-2C0 Digital I/O port 2C, port C on 82C55 no. 2

Base + 3: Digital I/O Configuration Register, 82C55 no. 1

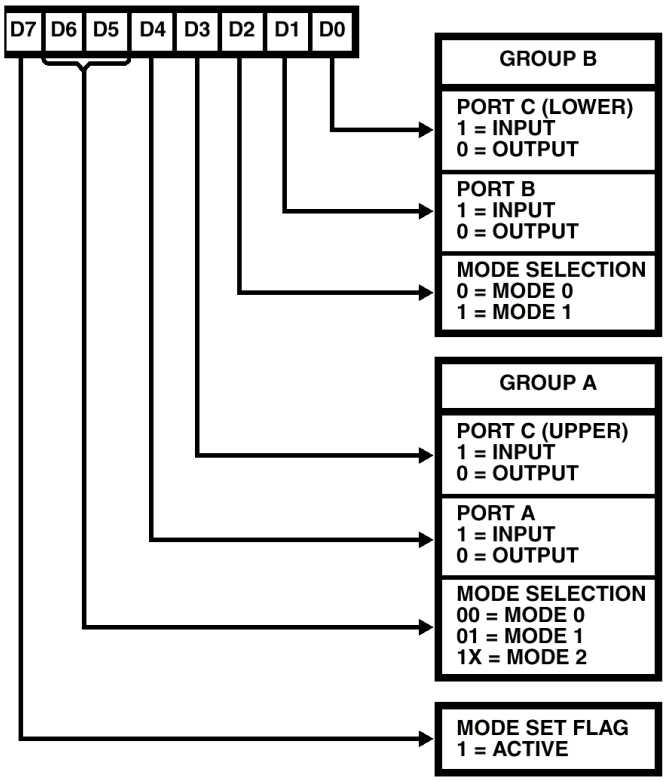
Base + 7: Digital I/O Configuration Register, 82C55 no. 2

These control registers determine the direction and mode of the 82C55 digital I/O lines. The diagram below comes from the 82C55 chip datasheet which is included at the back of this manual. Base + 3 is the control register for chip 1, and Base + 7 is the control register for chip 2.

Most applications use the simple I/O configuration in which bit 7 is set to 1 and the Mode is set to 0 for all ports.

Here is a list of common configuration register control bytes:

Configuration Byte				
Hex	**Decimal**	**Port A**	**Port B**	**Port C (both halves)**
9B	155	Input	Input	Input
92	146	Input	Input	Output
99	153	Input	Output	Input
90	144	Input	Output	Output
8B	139	Output	Input	Input
82	130	Output	Input	Output
89	137	Output	Output	Input
80	128	Output	Output	Output



7. Specifications

Digital I/O Circuitry

Chip	82C55A (x2)
Number of I/O lines	48
Direction	All lines programmable for input or output in groups of 4/8
Input voltage:	
Low	-0.5V min, 0.8V max
High	2.0V min, 5.5V max
Output voltage:	
Low	0.0V min, 0.4V max
High	3.0V min, Vcc - 0.4V max
Output current	±2.5mA max, each line
Pullup resistors	10KΩ all lines

General

Dimensions	3.550" x 3.775"
Power supply (Vcc)	5.0VDC ±10%, 200mA typical (all outputs open)
Card type	8-bit PC/104 bus compliant
Temperature range	-40 to +85^{o}C, operating and storage